

## **iCODING's DVB-RCS TURBO CODE CORE BOOSTS BROADBAND SATELLITE COMMUNICATIONS**

*Combination of new Xilinx FPGA and turbo codec core creates 35% increase for  
return channel broadband access via satellite*

**San Diego, CA** –December 20, 2001- iCODING Technology Incorporated announced a new broadband DVB-RCS (Digital Video Broadcast – Return Channel Satellite) compliant turbo decoder core that provides state-of-the-art Forward Error Correction (FEC) of up to 15 Mbits/sec on a Xilinx Virtex-II™ FPGA. The core can be used for Digital Video Broadcast (DVB), satellite communications, wireless LAN, digital TV, cable modem, and xDSL systems

iCODING's S2000 DVB-RCS Turbo Code core supports the new DVB-RCS standard (ETSI EN 301 790) that defines the return link for satellite based broadband interactive data services. iCODING is the first North American vendor to support the new Turbo Code FEC option, which provides a 35% increase in return channel efficiency over traditional concatenated coding schemes. The iCODING core enables rapid introduction of this technology into commercial systems furthering satellite's competitiveness with other broadband technologies.

"We are very excited about the interactive satellite market," says Brian Edmonston, iCODING's President. "With the throughput that is achievable using DVB-RCS on the uplink and DVB-S (Satellite) on the downlink, satellite providers can more than compete with traditional broadband providers for the 'last mile' solution."

The S2000 core is based on convolutional constituent codes and supports Quasi-Error-Free (QEF) performance on the return link. DVB-RCS is the second major standards body after 3G wireless to adopt convolutional-based turbo codes. These standards are adopting convolutional based turbo codes because they outperform all other FEC techniques. The core is also expected to be compliant with the emerging DVB-RCT standard for two-way Internet delivery via DVB-T (Terrestrial).

## **Leveraging FPGA Flexibility**

iCODING offers its S2000 intellectual property products to FPGA designers as ready to use, pre-tested cores through the Xilinx AllianceCORE and the Xilinx SignOnce IP License programs. These cores can be placed into Xilinx Virtex II and Virtex E FPGA's, allowing engineers to design, test, trouble shoot, and reconfigure leading-edge communication systems.

The use of FPGA's significantly reduces the time to test and develop wireless communications systems that must adapt to quickly changing broadband standards. This offers flexibility and savings that are typically not available with ASIC-based solutions. Datasheet information can be downloaded from the Xilinx IP Center website at: <http://www.xilinx.com/products/logicore/alliance/icoding/icoding.htm>.

## **S2000 Family of Turbo Codec Cores**

The S2000 Family of Turbo Codec Cores also includes the S2001 DVB-RCS Encoder, capable of 95 Mb/s on a Xilinx Virtex-II. The S2002 DVB-RCS Encoder and Decoder integrated and highly programmable. The S2100 DVB-RCT Decoder capable of data rates up to 31 Mb/s. The entire family achieves Quasi-Error-Free Performance, supports multiple modulation schemes, does not require external memory, and has low slice counts.

## **About iCODING Technology**

iCODING produces high speed and high performance FEC cores, was founded in 1999 and is headquartered in San Diego, California. As a leader in Turbo Coding Technology, for wireline, satellite, and 3G applications, iCODING is an active participant in the IEEE 802.16 standard, and the ITU. For more information on iCODING and Turbo Codes, visit the website at: <http://www.icoding.com>.

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