

### General Description

The iCODING S3016 Turbo Decoder implements the standard 3GPP™ universal mobile telecommunications system (UMTS), rate 1/3, 8-state PCCC turbo decoder. It uses a highly efficient architecture to minimise area and memory usage whilst still providing the high performance through the use of a full log MAP implementation, combined with good internal parameter scaling/quantisation. This is all at a data throughput of up to 2 Mbit/s.

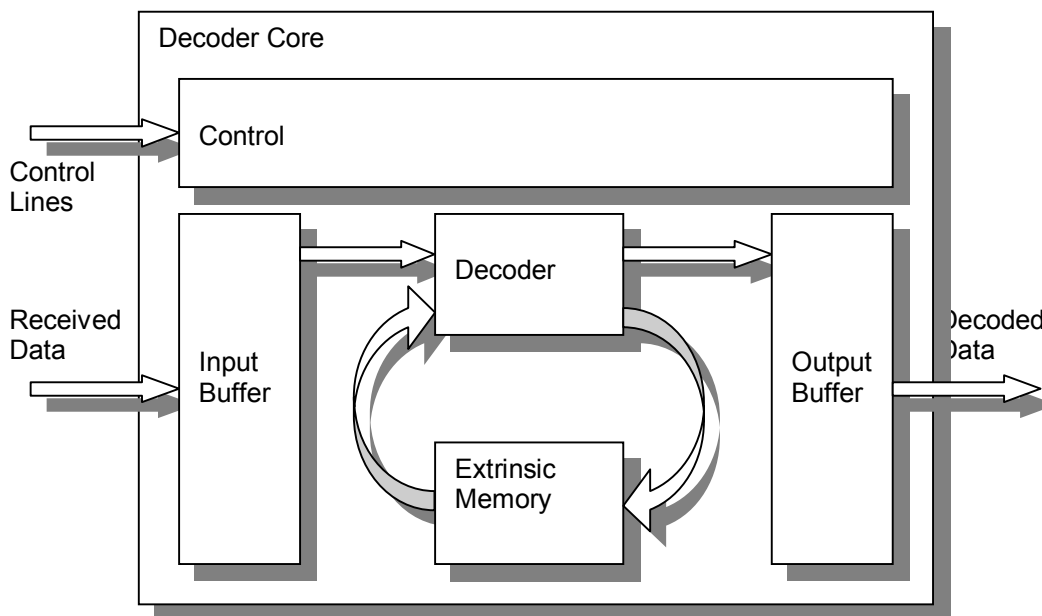
Control of the S3016 is performed via dedicated control pins, with frame settings updated on a per frame basis. Due to the framing signals used, frames can be input in a non-periodic manner if desired.

As with most iCODING products, the S3016 is customisable to meet different requirements either within the 3GPP-LTE specification by varying speed/area/performance tradeoffs or outside it, by varying such parameters as code rates, modulation and block sizes.

### Features

General features of the S3016 decoder include:

- Implements the full 3GPP-LTE™ standard Turbo Code
- Drop-in module for Altera Stratix II, Stratix III and Cyclone FPGAs
- No external memory required
- Implements a rate 1/3, 8-state PCCC turbo decoder.
- Frame sizes available from TBD bits, switchable on a per frame basis
- Programmable number of iterations (1 to 15), switchable on a per frame basis
- Supports data rates of 50 Mbit/s and 100 Mbit/sec at 6 iterations
- Max-Log MAP implementation
- 125 MHz clock rate
- Simple single clock operation



## Differentiators

The iCODING S3016 Turbo Decoder has the following features:

- Superior BER performance. Various algorithmic improvements provide materially superior performance.
- 100% internally generated interleavers for all frame sizes. No external calculation or parameter loading.
- Early stopping reduces iterations and power consumption.
- Very low clock-rate-to-data-throughput ratio.
- Automatic disabling of idle external memories.
- As much as half the gate count of other designs. Please contact for FPGA and ASIC gate counts.

## Deliverables

- Gate Level Netlist (FPGA)
- Synthesizable RTL Code (ASIC)
- Synthesis scripts (Design Compiler)
- Bit Exact C Libraries. Useful for generating test vectors.
- Test Bench and Vectors
- Complete Documentation

## Configuration

The S3016 is primarily available for Altera Stratix and Cyclone devices, but can be synthesized for alternative platforms. Please contact iCODING for further information.

For more information on this product, please contact



12463 Rancho Bernardo Rd #163  
San Diego, CA 92128  
USA  
Phone: +1-619-846-9276  
Fax: +1-253-763-8647  
E-mail: [info@icoding.com](mailto:info@icoding.com)  
[URL:www.icoding.com](http://www.icoding.com)