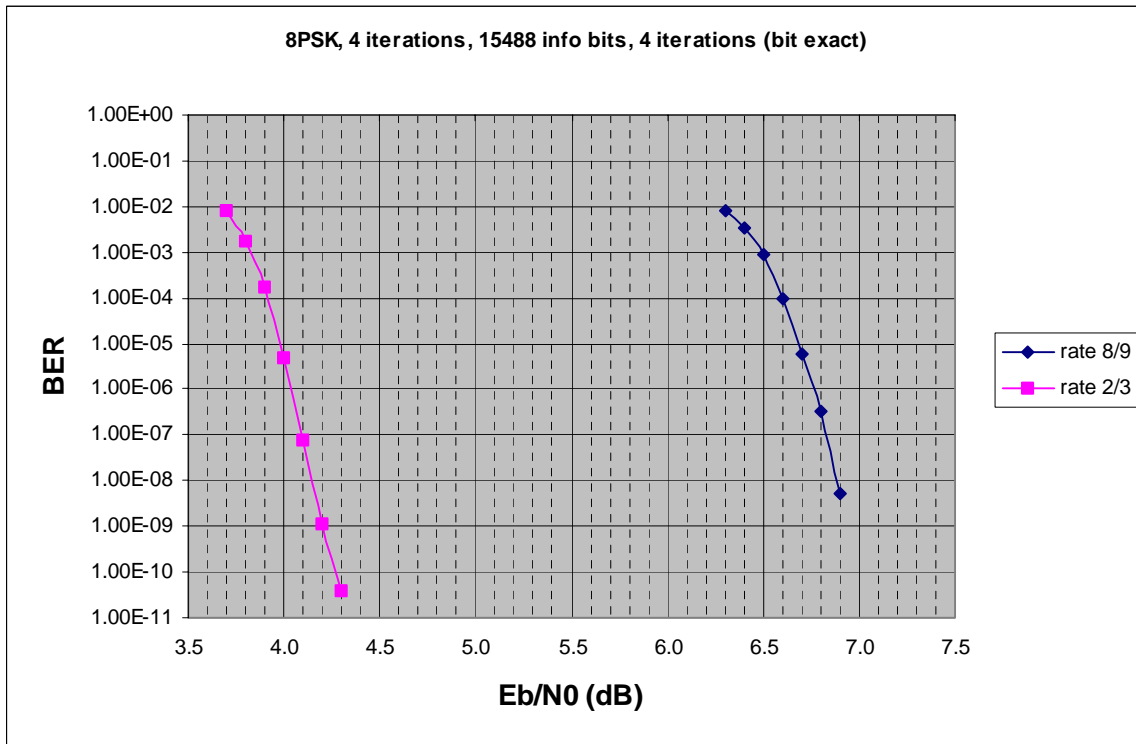


S1000 HIGH SPEED TURBO DECODER



8PSK 2.0 and 2.67 Bit/Sec/Hz

S1000 – Ultimate FEC and Flexibility

The S1000 decoder core combines the world's most powerful FEC with iCODING's ultra low error rate decoding schemes to provide maximum channel efficiency for your data transmission application.

The highly parallel broadband architecture brings the performance improvements of turbo coding to your high throughput communications application.

The S1000 synthesizes for Altera and Xilinx devices as well as ASIC, making it the ideal solution for your design.

Features of the S1000 decoder include:

- Data rates up to 15 Mbit/sec for 4 iterations in FPGA
- > 45 Mbit/sec in ASIC.
- Frame sizes up to 16 Kbits.

- No external memory needed in FPGA
- >3dB performance improvement over TCM
- Configurable to desired device, gate count, data rate and FEC performance
- QEF (BER<10-e10) performance
- Supports QPSK, 8PSK and 16QAM modes

iCODING's S1000 core can be configured for a wide range of coding rates, frame sizes and modulation schemes. Typically, only 4 iterations are required to obtain most of the performance benefits. However, additional iterations can typically increase performance by as much as .2 - .5 dB at the expense of data throughput. Turbo code performance also increases with frame size at the expense of latency and device cost.

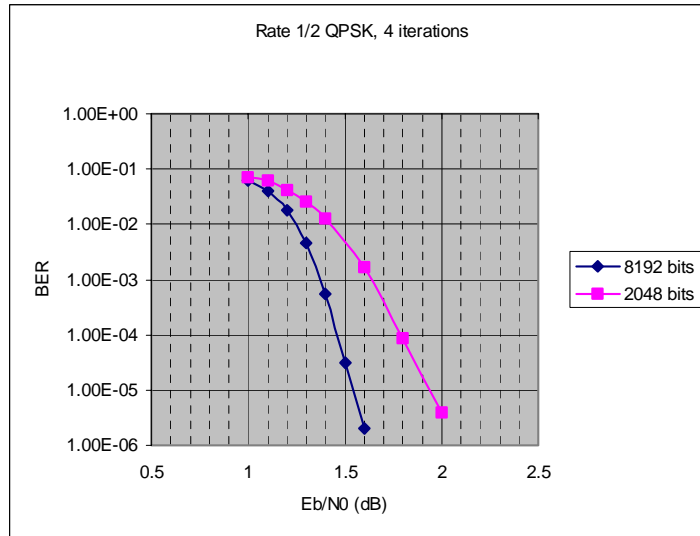
The S1000 provides QEF performance at both higher code rates and higher order



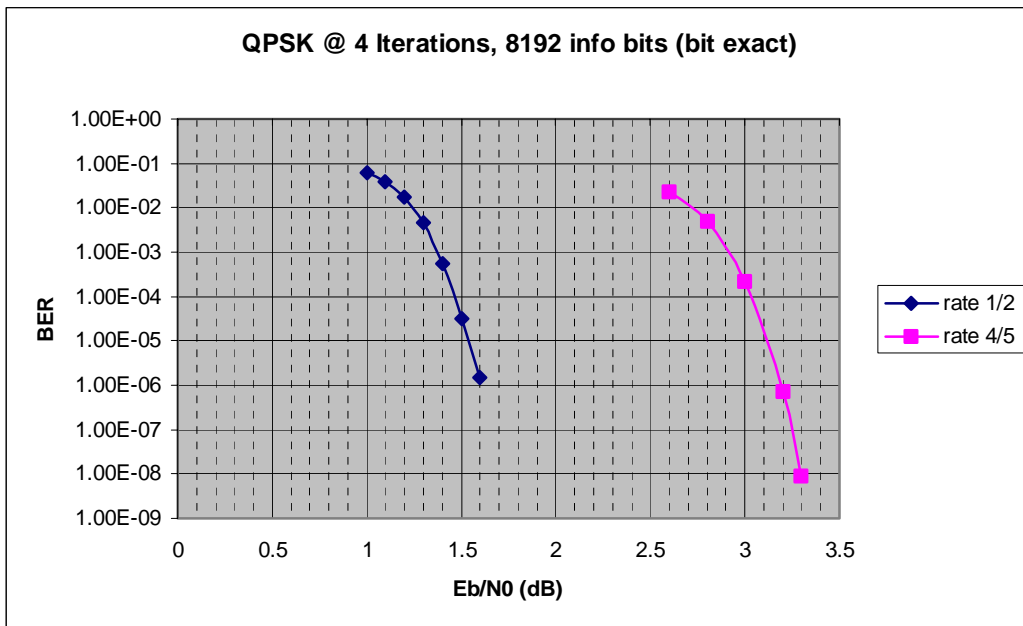
S1000 HIGH SPEED TURBO DECODER

modulation schemes. In default mode, the S1000 supports QPSK, 8PSK and 16QAM mode. Other modulation schemes can be included upon request. For additional

information please contact us at +1-619-846-9276.



Rate 1/2 QPSK for medium and large frame sizes.



QPSK 2048 information bits at rate 1/2 and 4/5.

S1000 HIGH SPEED TURBO DECODER

S1000 Specifications

Code Rates 1/2, 2/3, 3/4, 4/5, 5/6, 8/9

Mappings QPSK, 8PSK, 16QAM

Data Rate Up to 15 Mbit/Sec (FPGA) and 100 Mbit/sec (or higher) for ASIC
(Please contact us for most current speed information.)

Devices Supported

Xilinx XCV600E or higher

Altera EP20K300E or higher

* * *

iTERATIVE
iNNOVATION

The iterative decoding you have been waiting for™

Contact Information

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